CEO Perspective — *Innovation Requires IC Integrity*
Raik Brinkmann, President and CEO, OneSpin

I'm fascinated with cars, and there is a very famous car maker museum that I visited recently where they gave a thorough rundown of the history of each of their cars from how they are designed, to the materials they used, to the evolution of energy efficiency. It wasn't until the last exhibit where they talked about the future of automobiles and how AI, including machine learning, is the driving force behind the next several generations of cars and transportation in general. The exhibit went on to explain how each phase of autonomous learning will be exponentially more difficult than the one before. Each phase requires more significant "horse-power" in terms of data processing, how that data gets connected to everything else, and the customizations "under the hood" to the processors and SoCs.

Looking around, I noticed that most people didn't seem to fully grasp this significance. And I understand why. We live in a world where we often take for granted that our electronic devices work as we expect. Moreover, we often don't think about whether devices are safe or secure. We don't care about the complexities involved with making the chips that power our devices. We simply just want our devices to run and trust that they won't have issues. For better or worse, we as consumers are justified in our attitude.

Companies designing our electronics have an obligation to meet functionality, safety, and security requirements or they are met with swift ramifications. We've all seen the headlines when something catastrophic happens, whether it be a plane crash, car crash, or a malicious hacker attack. Once that occurs, consumer trust is eroded and difficult to get back. Issues don't have to be headline making to be devastating to a company's bottom line. Turning out a product that has unknown performance or power issues, for example, can spell doom when detected in the field.

Meeting these requirements becomes tougher and tougher as innovation progresses, however. The SoCs that empower 5G, IoT, and AI that are at the crux of today's innovation have to be increasingly complex, often with seismically bigger capacity and power, and the ability to be more flexible and customized. This up-shift means that companies have to be hyper-diligent not only about the functional correctness of their designs but also the safety, trust, and security. The design must operate as intended in even the most adverse environmental conditions and be immune to any unwarranted interference. To say it concisely, companies must be fully invested in the entire integrity of their IC – functional correctness, safety, trust, and security.

Take, for example, XL chips (multi-billion gate chips) and heterogeneous computing platforms. The adoption of these has become a significant trend in order to implement today's applications. XL chips contain millions of connections, over 60 million module instances, and over 30 thousand modules. Further, they contain multiple CPUs, programmable logic accelerators, and third-party IP, and are software programmable. Add to all this the customization that is needed for these environments to compete, and you can see that the complexity is astounding, and verification of these systems can be daunting.

Heterogeneous environments are being used more and more in such industries as automotive, aerospace, and industrial where functional safety and security seem to be critical additions to making sure the design functions correctly. Understanding the different types of faults and how they impact the design is paramount. Many of these designs must also comply with stringent safety standards such as ISO 26262 or DO-254. Designers must contend with these requirements as well.

A complete verification that takes into account IC integrity standards starts with thorough verification planning that includes documenting the requirements of design and verification, including writing specific assertions. Getting to complete coverage is a challenge in any environment. You typically use multiple technologies to perform verification (e.g. simulation, emulation, and formal) but without the convergence of these technologies into a single view, understanding where the holes are in your coverage is extremely difficult.

The ability to verify that the millions of connections are working properly is of course critical. The use of simulation can only get you so far and can be inefficient even in less complex scenarios. What's needed is an exhaustive verification approach technology that can handle the huge number of connections. At OneSpin, we worked closely with our customer Xilinx to address this challenge when others couldn't. You can read more about it in a joint conference paper presented at DVCon. (http://bit.ly/OneSpinWhitePaper)

Equivalence checking is another issue. In a heterogeneous environment, you must ensure that you have achieved equivalence of the RTL through ASIC/FPGA synthesis to the final netlist. Simulation and emulation can't perform this function. This is a very specific task that can only be achieved with unique formal solutions.

If we take a closer look at artificial intelligence (AI) chips that power machine learning (ML) and deep learning (DL) applications, most include floating-point units (FPUs). Algorithms used in neural networks often use multiplication and addition of floating-point values. In particular, convolutional neural networks (CNNs), popular for computer vision applications, may involve deeply nested loops of floating-point operations, which subsequently need to be scaled to different sizes in order to meet the precision and area requirements. There is significant value in the use of FPUs, but it means increased importance must be placed on thoroughly verifying floating-point hardware including ensuring the complex IEEE 754 floating-point standard is being met. Once again, simulation falls short in this capacity. At OneSpin, we've developed a formal technology that can achieve 100% coverage and compliance to the standard. You can download our case study on this topic. (http://bit.ly/OneSpinWhitePaper)

When it comes to safety, you need to start verification analysis by doing some FMEDA (failure modes, effects and diagnostic analysis) to map out the different types of faults that will have a negative impact on the function of the design. You need a plan on how to cover these faults and you need to accurately measure how well you've done. With regards to complying with stringent safety standards, using verification solutions that are already safety certified and working with a verification partner to guide you through the certification process can shave a significant amount of time and effort.

Security and trust can be approached using advanced formal techniques in a similar manner as verifying functional correctness. But to verify if a design is secure and trusted, you must prove the absence of additional design logic and the absence of modifications to the design flow. You must determine that the design is fully compliant with its outlined specification and certification.

At OneSpin, we're committed to helping our customers deliver worry-free electronics - devices that work as intended and free of safety and security concerns. To do that we are committed to assuring that IC integrity standards are being met when developing functionally correct, safe, trusted and secure designs. We work closely with our customers to make sure that we're providing solutions that fully verify the complex dimensions if IC integrity. Being able to meet the worry-free expectation that the world demands is crucial for continued innovation.

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Connecting Design to Manufacturing
Bob Smith, Executive Director, ESD Alliance, A SEMI Strategic Association Partner

You can expect to hear much more from the ESD Alliance in the coming months about our "Connecting Design to Manufacturing" campaign. We're taking on long-held perceptions that differentiate design from manufacturing and treat them as two distinct areas pursuing different objectives, even though they are part of the same semiconductor supply chain.

The ESD Alliance is almost perfectly positioned to change or expand your perception of the semiconductor supply chain and the electronic system design ecosystem's role within it, especially as a SEMI Strategic Association Partner. Connecting Design to Manufacturing also neatly ties into SEMI's own "SEMI is More" campaign.

With much more of a global presence under the SEMI umbrella, we have a greater range as the central voice of the semiconductor design industry. We can promote the electronic system design ecosystem's value as a vital component of the global electronics product manufacturing supply chain and take on a campaign to "Connect Design to Manufacturing."

As noted in several other articles in this newsletter, "Connecting Design to Manufacturing" began rolling out in September at SEMICON Taiwan with the first Smart Data Global Summit sponsored by member companies Cadence and Synopsys. An executive-level industry meeting where we discussed common industry issues and bottlenecks that could be addressed through collaboration also in Taiwan followed. We're discussing similar types of events at other SEMICONs.

SEMICON® TAIWAN

November is SEMICON Europa in Munich, Germany, and the ESD Alliance unveils SMART Design, the first system-centric series showcasing advances in electronic system design to be held at the event. SMART Design's program, "Designing Electronic Systems for Future Applications," features a series of presentations and a panel discussion highlighting how advances in electronic system design are enabling emerging and future applications.

Also debuting at SEMICON Europa is the SMART Transportation Forum led by SEMI's Global Automotive Advisory Council (GAAC) with presentations from the design, semiconductor equipment and materials suppliers and automotive OEM communities. "Connected-to-Everything Automated Mobility," including talks from members of the EDA, design, automotive and fab ecosystems, a further example of "Connecting the Divide."

Another milestone is the celebration of the 25th Phil Kaufman Award. This year's recipient is Dr. Mary Jane Irwin, the first woman recipient who is noted for her contributions to EDA via her technical efforts, service to the community and leadership. She is the Evan Pugh Professor and A. Robert Noll Chair Emeritus in Engineering in the Department of Computer Science and Engineering at Penn State.

Our move into SEMI gives the electronic system design ecosystem greater insight into the challenges and opportunities within the full semiconductor supply chain. And, we are working to give the manufacturing community similar insight into the challenges from the design ecosystem. We have much more, however, to do to "Connect Design with Manufacturing.

We welcome any ideas or suggestions from you to help us "Connect Design to Manufacturing.

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Committee Updates

Export (Larry Disenhof, Cadence Design Systems). The Export Committee continues to monitor government activities and rulings that might have a significant impact on your business.

As I reported in the last newsletter this continues to be a very busy time in the trade compliance world, and it's important to keep updated on the latest news coming from the U.S., EU and China.

In Europe we are waiting on updates to the EU export regulations where we expect new rules on controls on cyber-security surveillance technology, language on human rights and international humanitarian law and a harmonized interpretation of key concepts on such areas as cloud computing and transfers of technology. And don't forget Brexit – if it happens and you currently ship into/from the UK and the rest of the EU, you need to ensure you have updated license permits in place.

In the U.S. we still await the Commerce Department's (BIS) Advanced Notice of Proposed Rulemaking (ANRPM) on *Foundational Technologies*, which might include a proposal to review EDA for stricter levels of export restrictions. We expect the ANPRM before year-end, with a 60-day response time. Committee members will be coordinating a response once we see the scope of the ANPRM.

License Management & Anti-Piracy (LMA) (Sashi Subramanian, Cadence Design Systems). The LMA committee continued to hold regular meetings to discuss matters of common interest.

The LMA committee continued to hold regular meetings to discuss matters of common interest. We finalized the Joint Development Agreement for the Machine Certification project with the Development Partners. The document is currently waiting for approval and signature from each of the Development Partners. The committee also continued engagement with Flexera on improving the license server capacity to support large transaction volumes, currently a limitation for the FlexNet license server.

Interoperability (Richard Paw, Amazon Web Services). As the Electronic Systems Design market continues to evolve, the Interoperability Committee continues to explore factors that could impact the operation or the interoperability of electronic system design tools or IP.

The ESD Alliance OS Roadmap represents industry guidelines regarding operating system versions that EDA vendors should publish against and customers should use for new designs. The "Max version for vendors" indicates the latest OS version vendors should use for software releases. "Min version for users" indicates the oldest OS version that customers should consider when starting a new design.

Based on meetings and discussions of the status of common EDA operating systems, the committee has decided to mark RHEL 6 as deprecated. This indicates that RHEL 6 support is expected to end soon and customers are urged not to start new designs on RHEL 6. As a reminder, SLES 11 was deprecated earlier this year. New designs and development should be using RHEL 7 or SLES 12. As always, you can find the latest OS Roadmap on the ESD Alliance website, esd-alliance.org.

Market Statistics Service (MSS): (Paul Cohen, SEMI). The ESD Alliance's [MSS report](#) captures EDA, semiconductor IP and services revenue data reported in complete confidence by companies providing these products and services and organizes it into a published report available to members. The most recent report, covering through Q2, 2019, shows quarterly industry revenue up 6.6% compared to Q2, 2018 on revenues of $2.5 billion, with the 4-quarter moving average up 6% The report includes historical revenue data by quarter organized by detailed product categories (chart) and geographic regions. The report provides valuable data to help guide member companies' business decisions. Additional information including the MSS Newsletter is available at [esd-alliance.org](#).
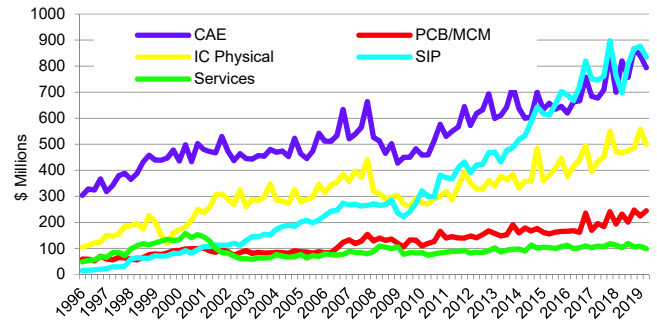
Emerging Companies (Julie Rogers, SEMI). The Emerging Companies Committee continues to hold informative events on topics of interest to the system and semiconductor design ecosystem.

The Emerging Companies Committee is busy planning events for 2020, including the popular Jim Hogan Fireside Chat series, where he interviews entrepreneurs about their experiences building successful companies in the electronic system design ecosystem. We're also planning the 2020 installment of the popular CEO Outlook.

In fall 2019 we attended SEMICON Taiwan and SEMICON Europa, where we began discussions with other SEMI regions to bring valuable educational and networking activities to locations outside of Silicon Valley.

As always, recordings of past events are available in the ESD Alliance Resource Center.

Be sure to visit the ESD Alliance website, esd-alliance.org, and the SEMI website for details of upcoming events as they become available.

Tradeshow (Bob Smith, SEMI). The committee represents the interests of ESD Alliance companies at trade shows including SEMICON West, Design Automation and Test Europe (DATE), SEMICON Europa, SEMICON China, and others.

Now that the ESD Alliance is a SEMI Strategic Association Partner, we have been busy expanding our reach beyond North America, including new events at SEMICON shows around the world.

In September, we hosted the Technology Think Tank Summit at SEMICON Taiwan, that gathered global industry leaders to share opinions and visions of the industry future. Another event was the Smart Data Global Summit Forum, sponsored by Cadence and Synopsys. It features talks on Artificial Intelligence and ubiquitous computing in the digitally transformed future from Arm, Cadence, Facebook, Mentor, a Siemens Business, Qualcomm and Synopsys. Additionally, the ESD Alliance hosted an industry meeting to outline its development plans and practice sharing.

We continue to expand our global activities at SEMICON Europa, November 12 – 15 in Munich, Germany. This year, SEMICON Europa includes "SMART Design," sponsored by OneSpin and Onscale, featuring presentations and a panel discussion highlighting how advances in electronic system design are enabling emerging and future applications.

ESD Alliance at SEMICON Taiwan

SEMICON Taiwan was held September 18 through 20 at the Taipei Nangang Exhibition Center in Taipei, Taiwan.

The ESD Alliance hosted a number of events at SEMICON Taiwan, including the "Smart Data Global Summit", featuring talks and a panel covering design and verification for AI. The summit, sponsored by Cadence and Synopsys, featured talks from Shahriar Rabii (Facebook), Wally Rhines (Mentor, a Siemens Business), Way Sing Lee (Qualcomm), Paul Cunningham (Cadence), Ian Smythe (Arm), and Susheel Tadikonda (Synopsys). Following the talks, the speakers gathered for a panel moderated by Yu-Chin Hsu (Ministry of Science and Technology).

Following the summit, the ESD Alliance hosted a VIP Reception, attended by many of the panelists and others.
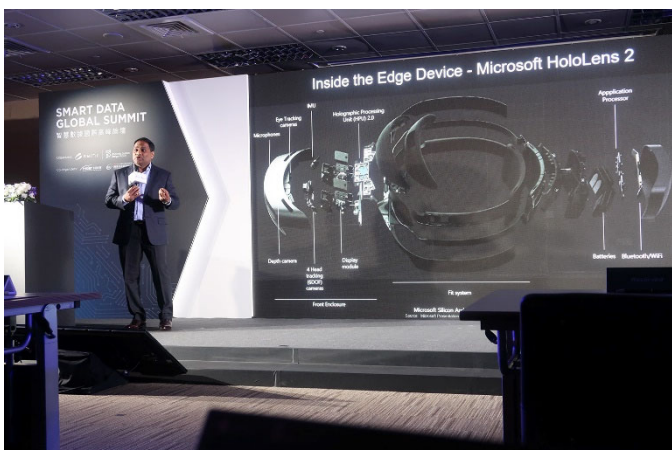
For more information about ESD Alliance events, visit the Resource Center at esd-alliance.org.

Bob Smith, Executive Director of the ESD Alliance, introduces the Smart Data Global Summit at SEMICON Taiwan

Wally Rhines, CEO Emeritus of Mentor, a Siemens Business, talks about how AI is driving the next generation of computing and IC design.

Susheel Kadikona, VP of Engineering in the Verification Group at Synopsys, talks about AI on the edge.

Following the talks, the speakers gathered for an informative panel session moderated by Yu-Chin Hsu, Deputy Minister at the Ministry of Science and Technology.

ESD Alliance at SEMICON Taiwan

SEMICON Taiwan was held September 18 through 20 at the Taipei Nangang Exhibition Center in Taipei, Taiwan.

SEMICON Taiwan's tag line, "Leading the Smart Future," was evidenced in one of the first sessions on Wednesday, September 18. The E-innovation Forum included talks on the future of technology, including "Technology Node – What is in a Name" by H.S. Philip Wong (TSMC), "Singapore's Innovation and Enterprise Plan 2015 – 2020 by Teck Seng Low (National Research Foundation, Singapore), and "Our Future is About Technology and Choices" from Luc Van den Hove (IMEC). "The New Path for Edge AI" was covered by Emmanuel Sabonnadiere (CEA-Leti), while Alex Y.M. Peng (ITRI) presented "Go Beyond the Valley of Death via OISP."
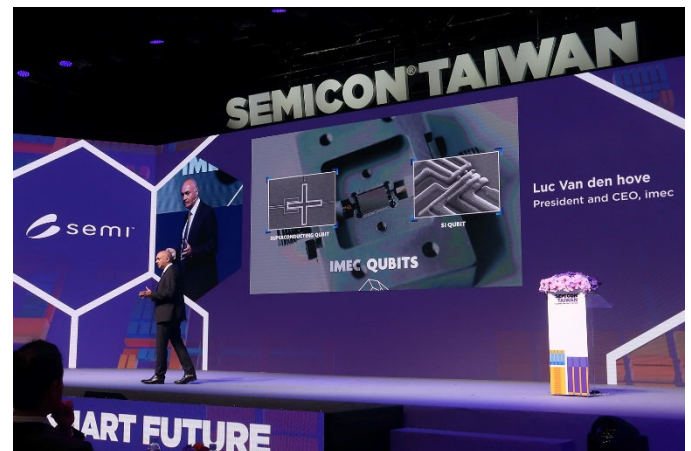
Following the talks, Chenming Hu (UC Berkeley and recipient of the ESD Alliance's 2013 Phil Kaufman Award) moderated a panel including the speakers.

The ESD Alliance also conducted the first "ESD Alliance Industry Meeting", where local representatives from EDA, SIP, and design companies gathered to discuss how ESD Alliance activities can expand and benefit the Taiwan semiconductor design ecosystem.
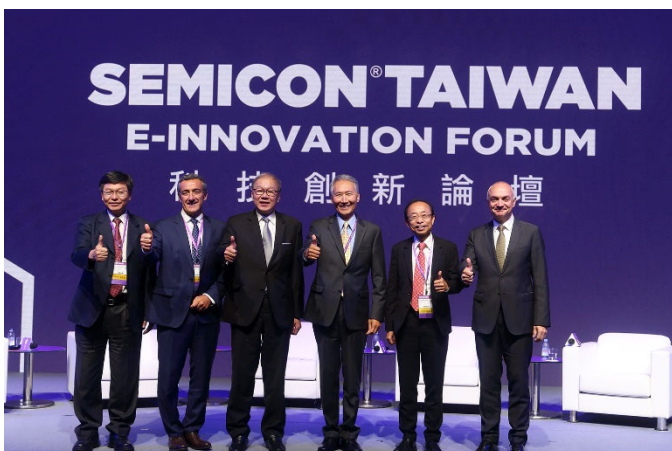
For more information about ESD Alliance events, visit the Resource Center at esd-alliance.org.

TSMC Vice President H.S. Philip Wong discussed the future of technology nodes at the E-innovation Forum.

IMEC's President and CEO, Luc Van den Hove, talks about future technology and choices.

Following the talks, the speakers gathered for a panel session moderated by Chenming Hu, Professor Emeritus at UC Berkeley and recipient of the ESD Alliance 2013 Phil Kaufman Award.

Taiwanese representatives of major EDA, SIP, and design companies gathered to discuss how ESD Alliance activities can benefit the Taiwan semiconductor design ecosystem.